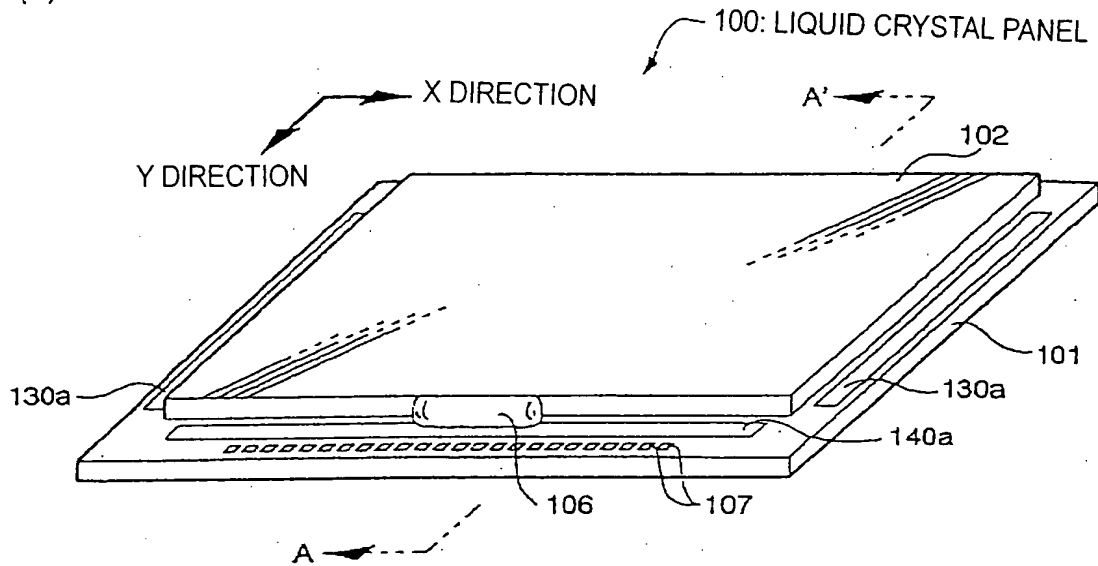


FIG. 1

(a)



(b)

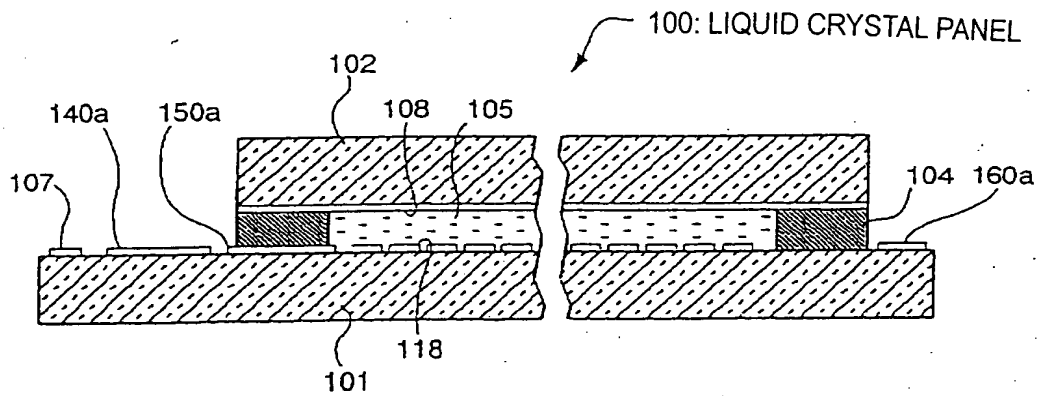


FIG. 2

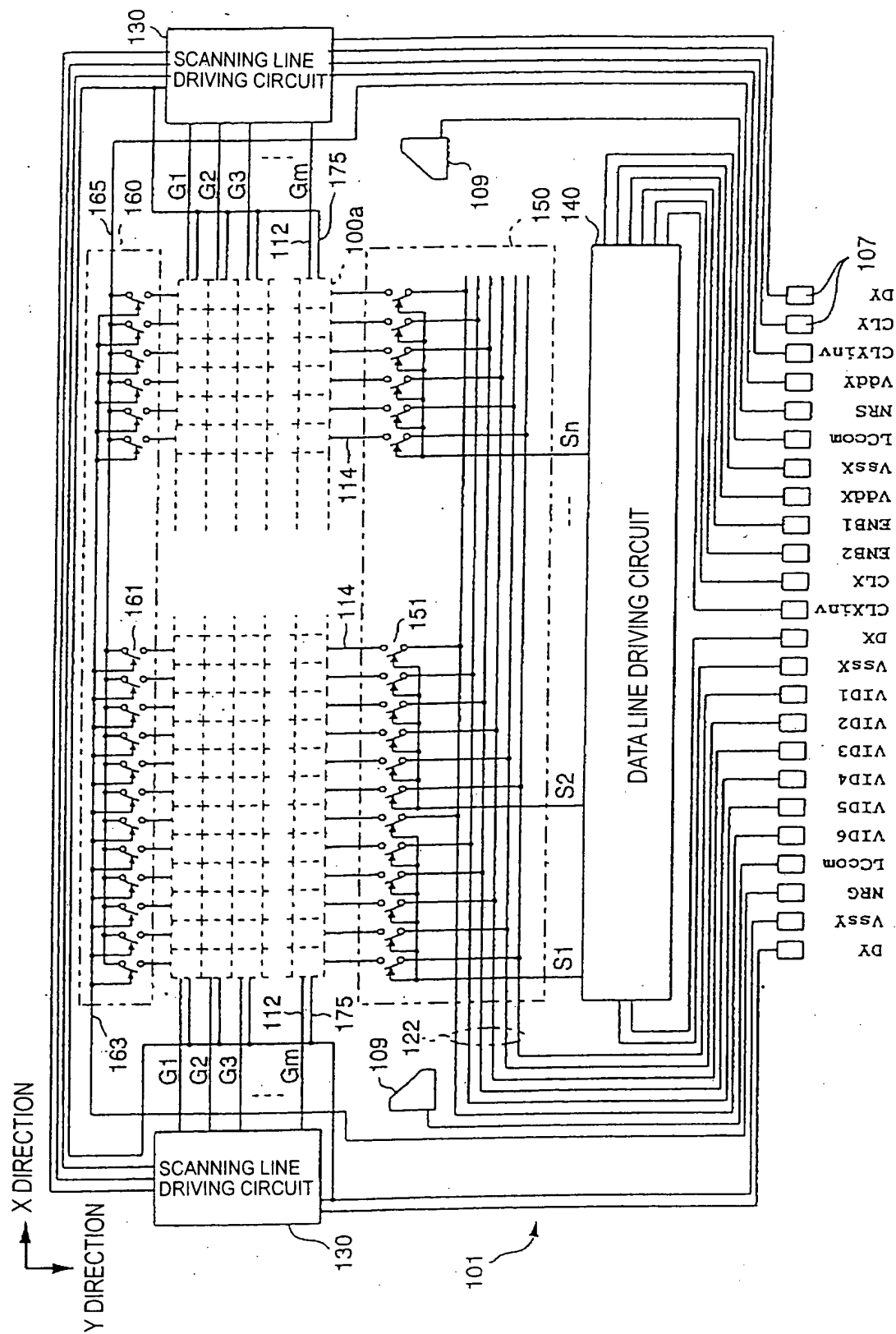
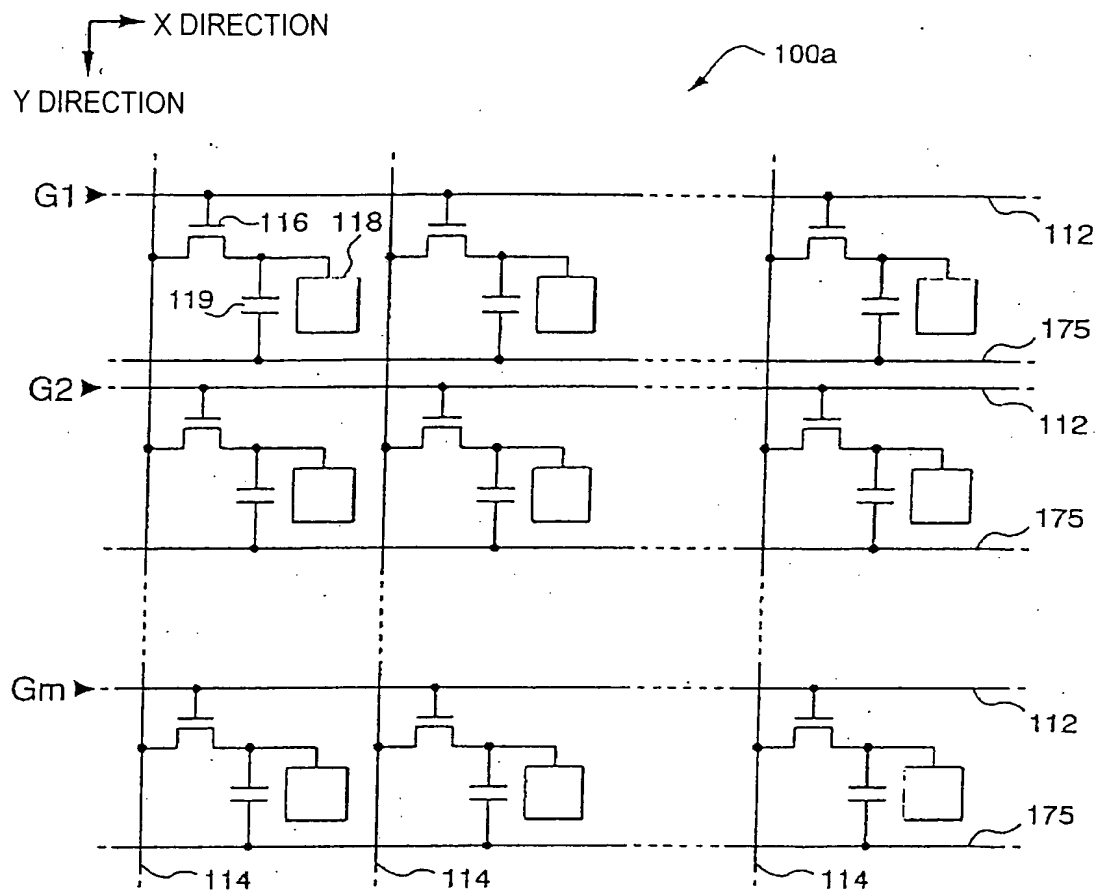


FIG. 3



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FIG. 4

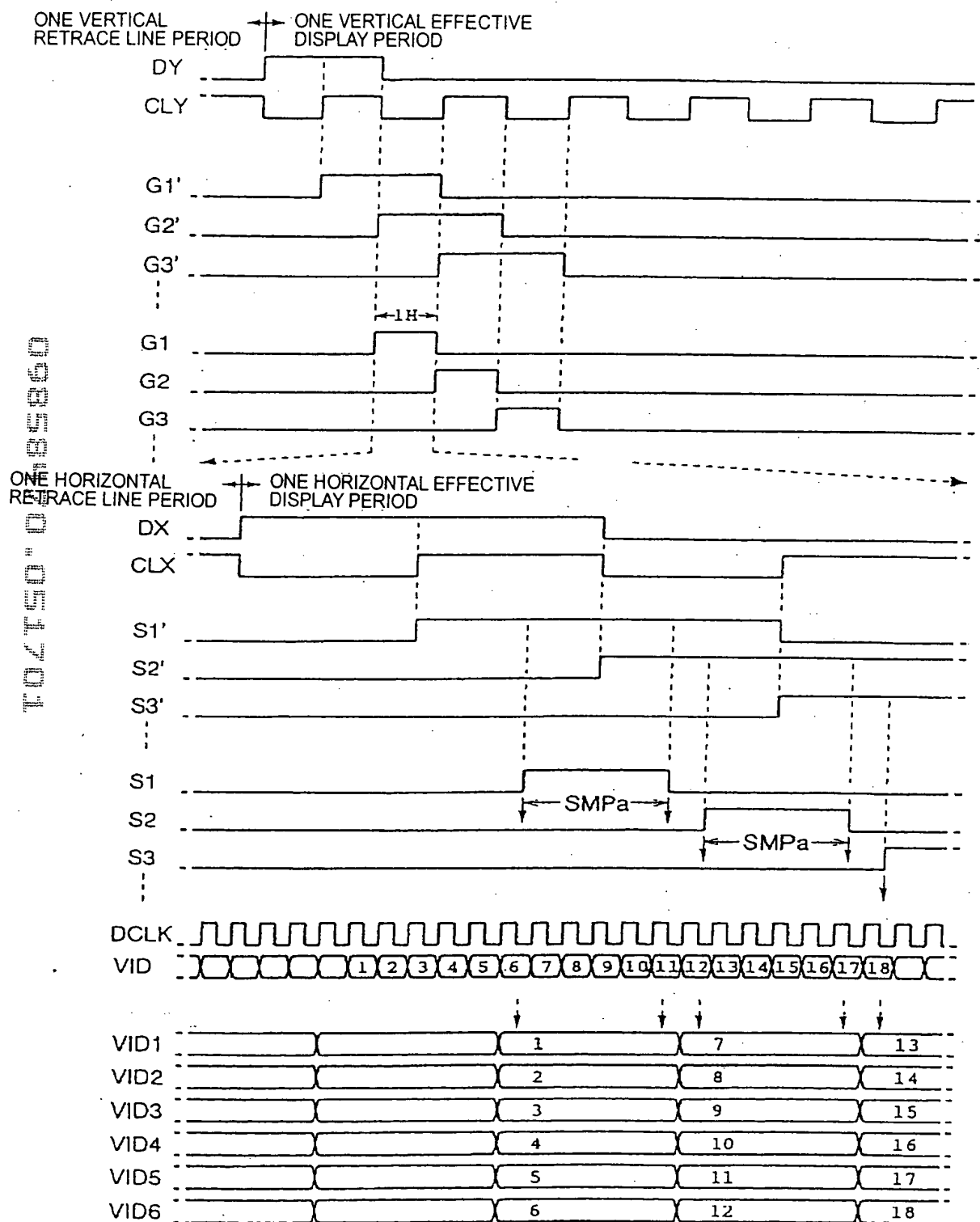
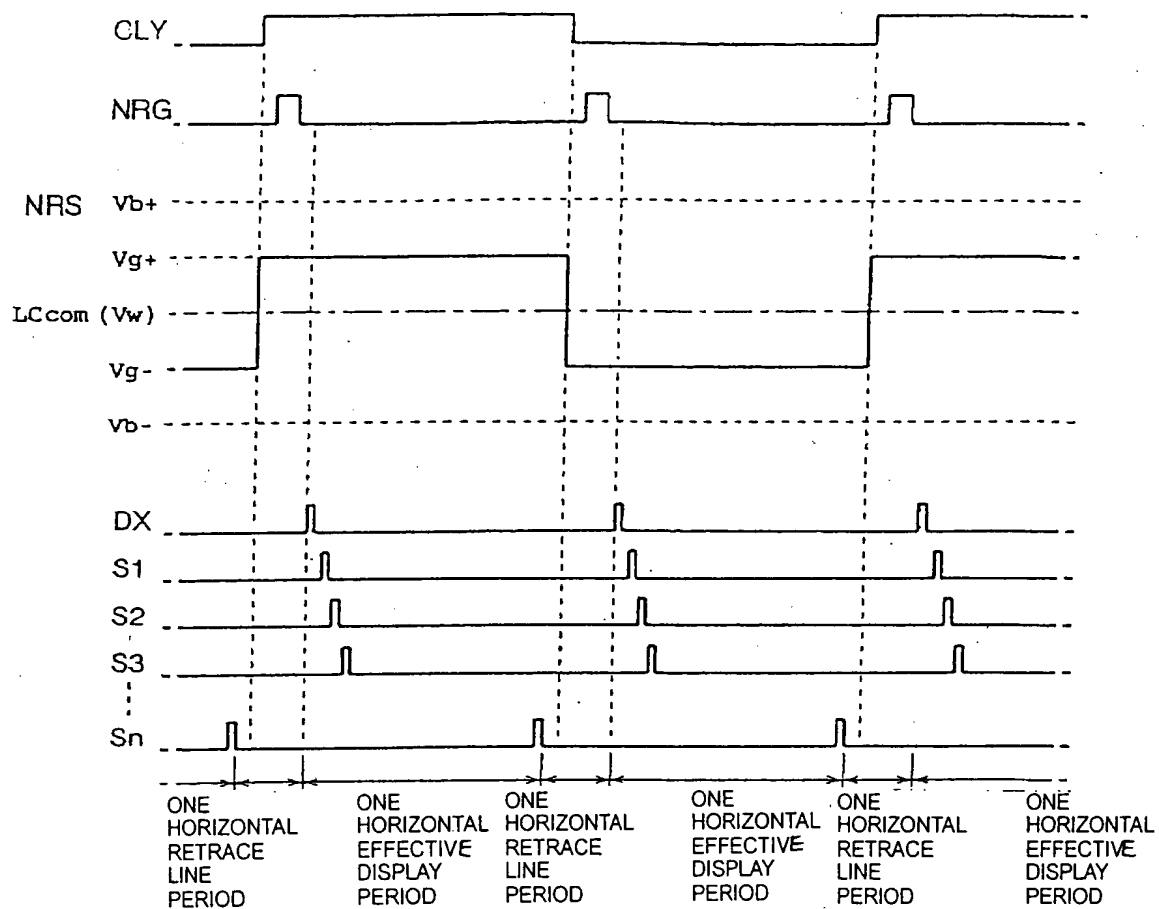
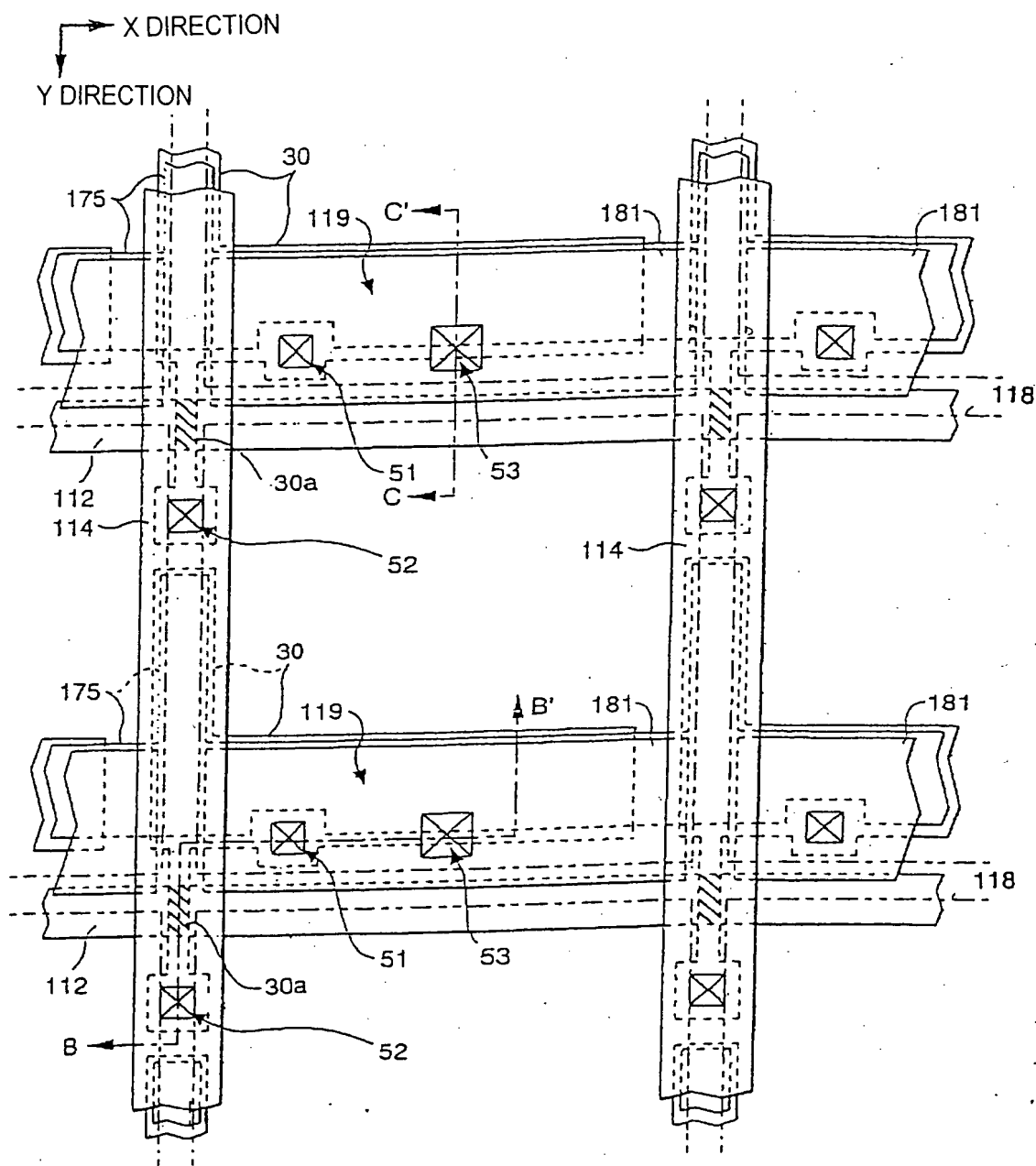


FIG. 5



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FIG. 6



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FIG. 7

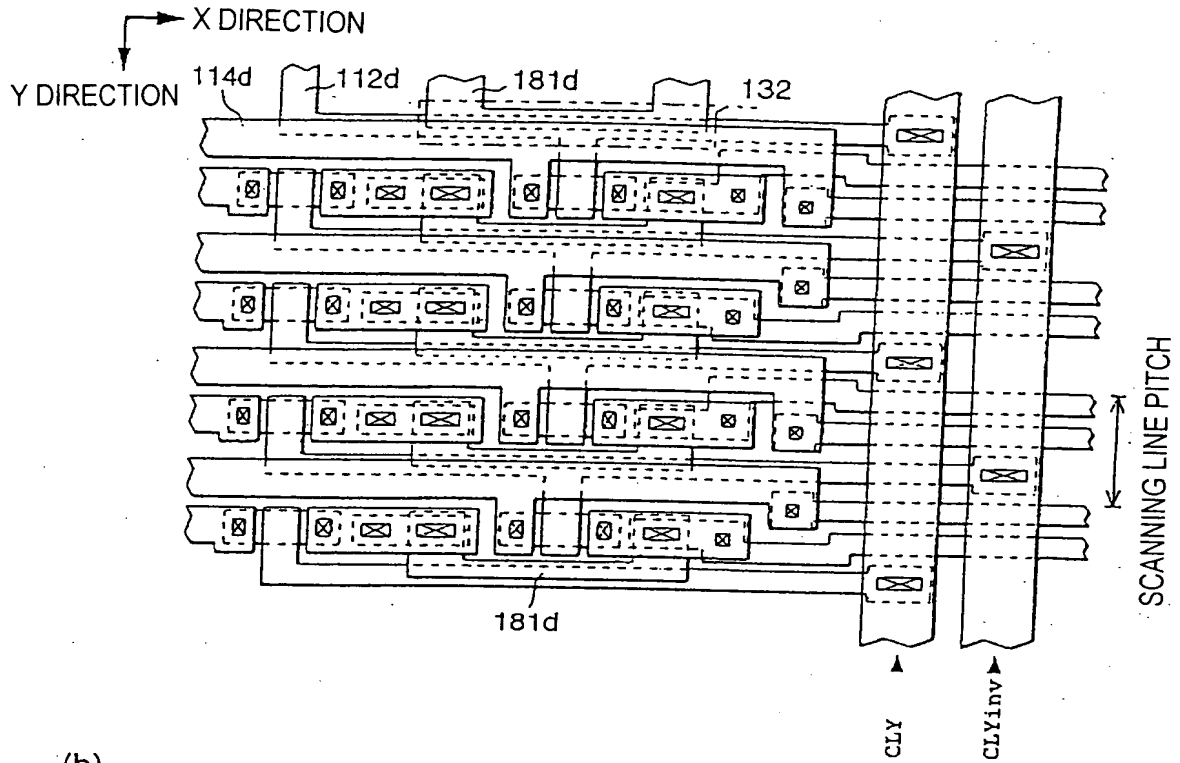




TOP SECRET 0485860

FIG. 9

(a)



(b)

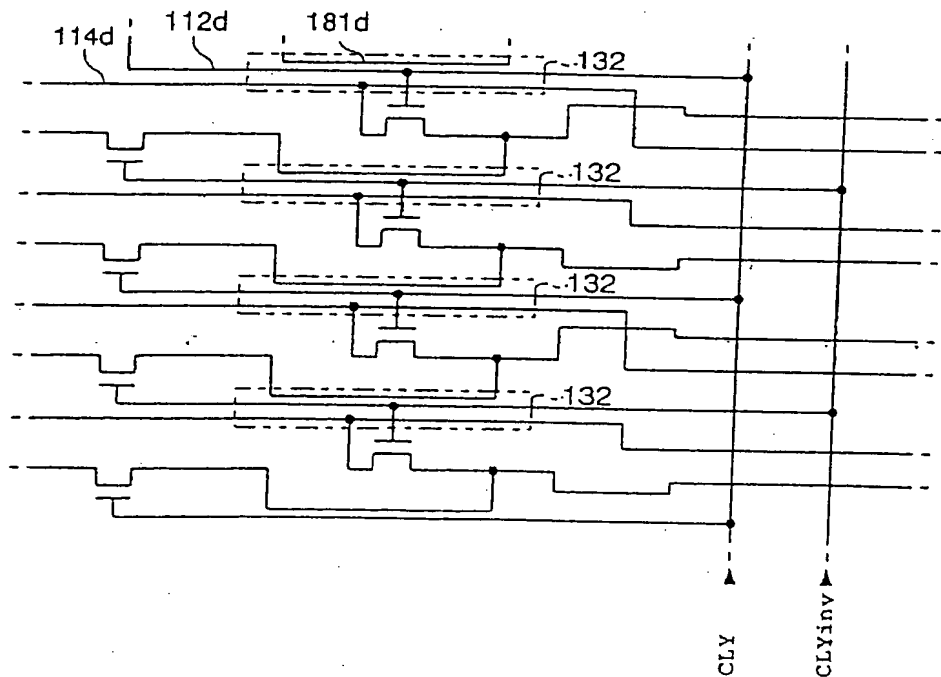
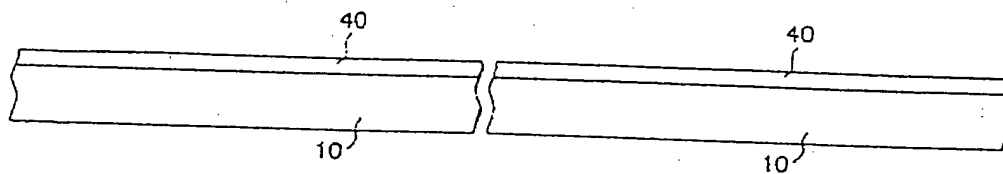


FIG. 10 |

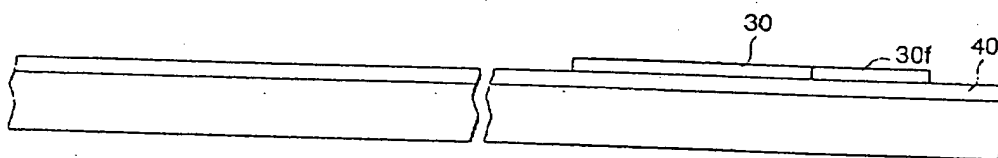
(1)

PERIPHERAL CIRCUIT REGION

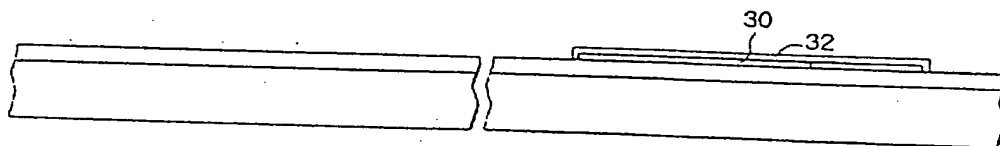
DISPLAY REGION



(2)



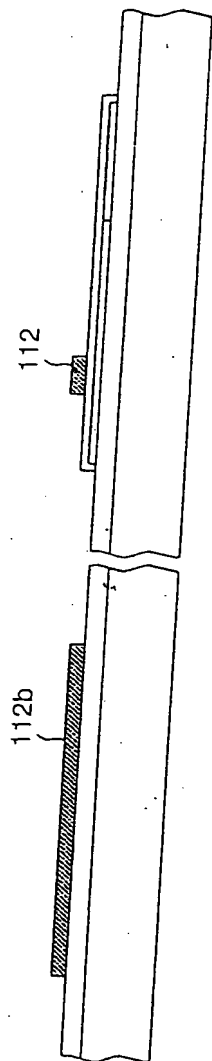
(3)



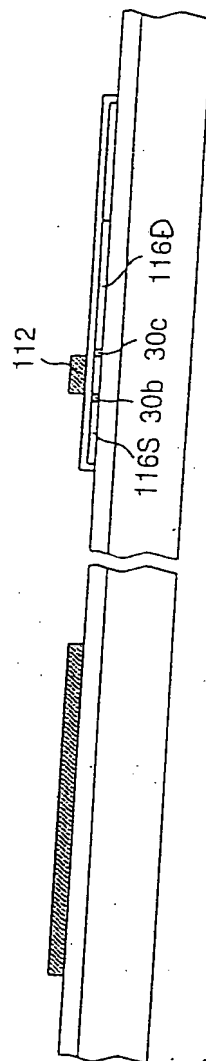
09858470.051701

FIG. 11

(4)



(5)



(6)

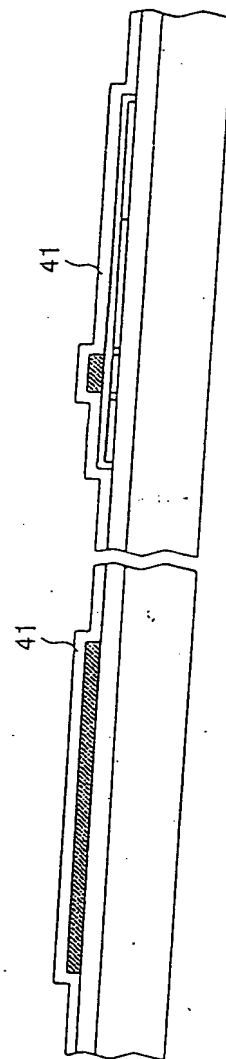
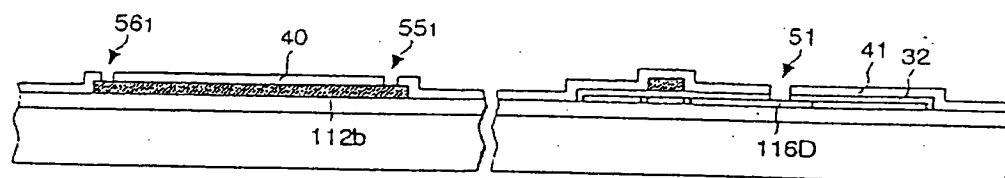
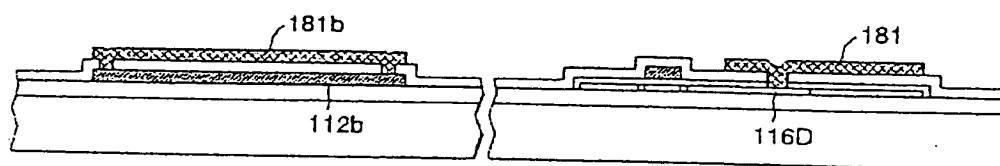


FIG. 12

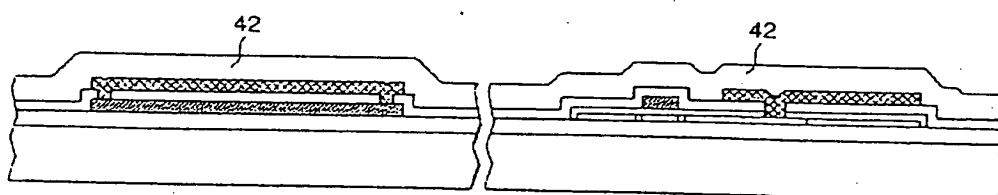
(7)



(8)



(9)

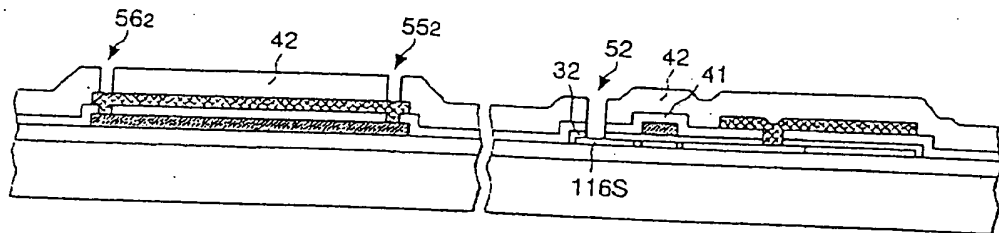


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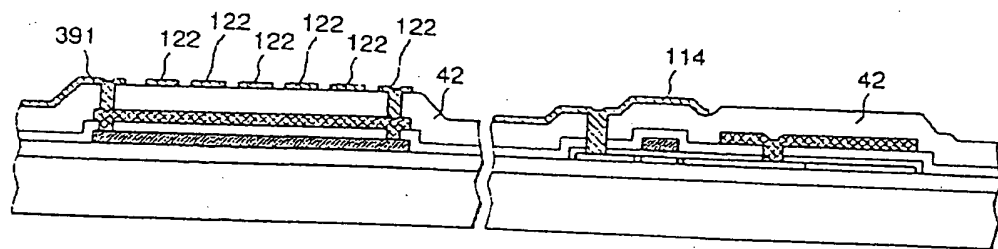
09558470.051701

FIG. 13

(10)



(11)



(12)

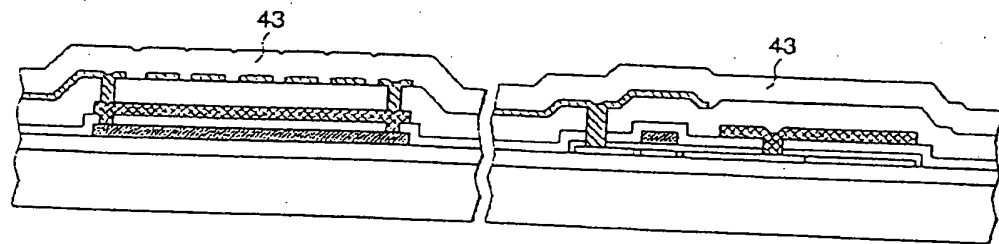
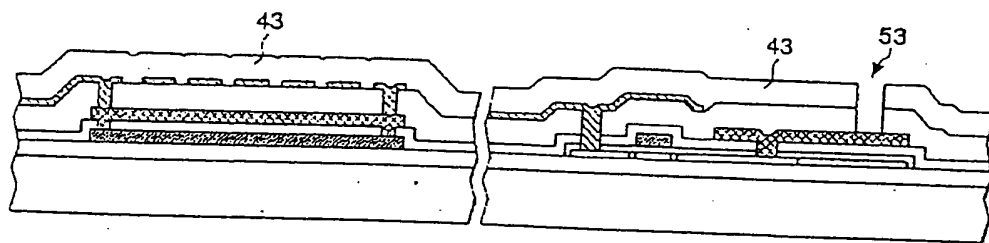


FIG. 14

(13)



(14)

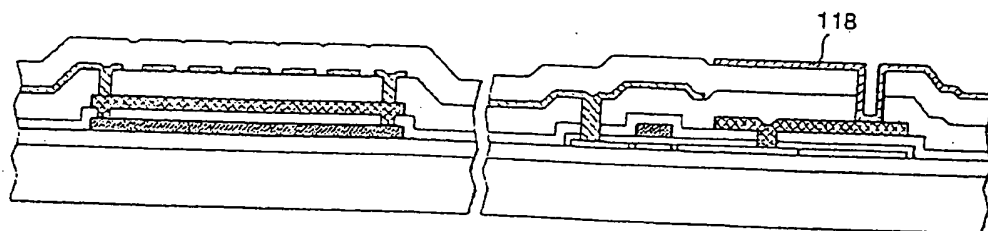
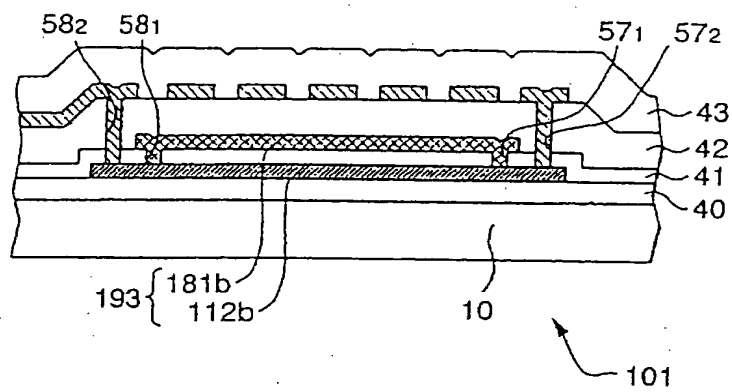
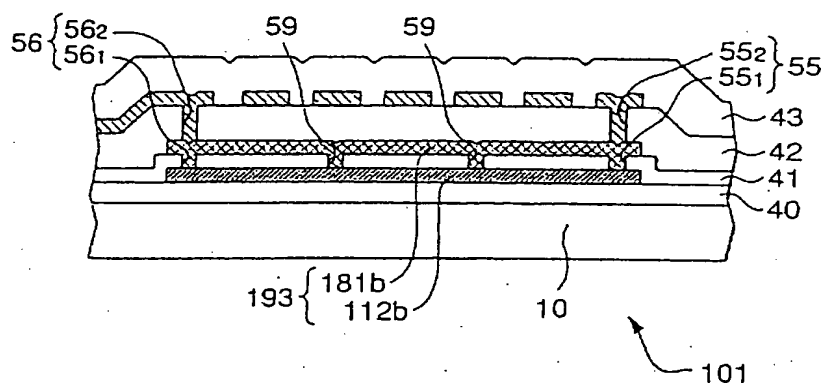


FIG. 15

(a)



(b)



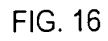
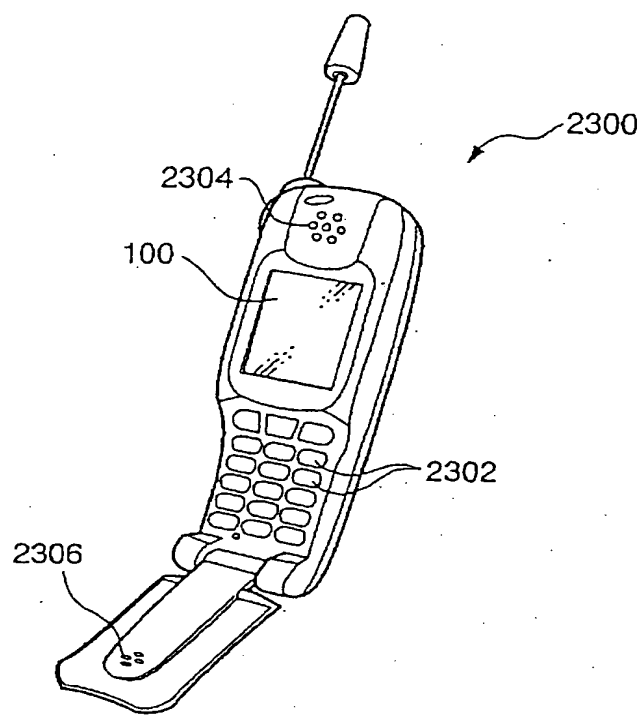


FIG. 18



0985470.051701